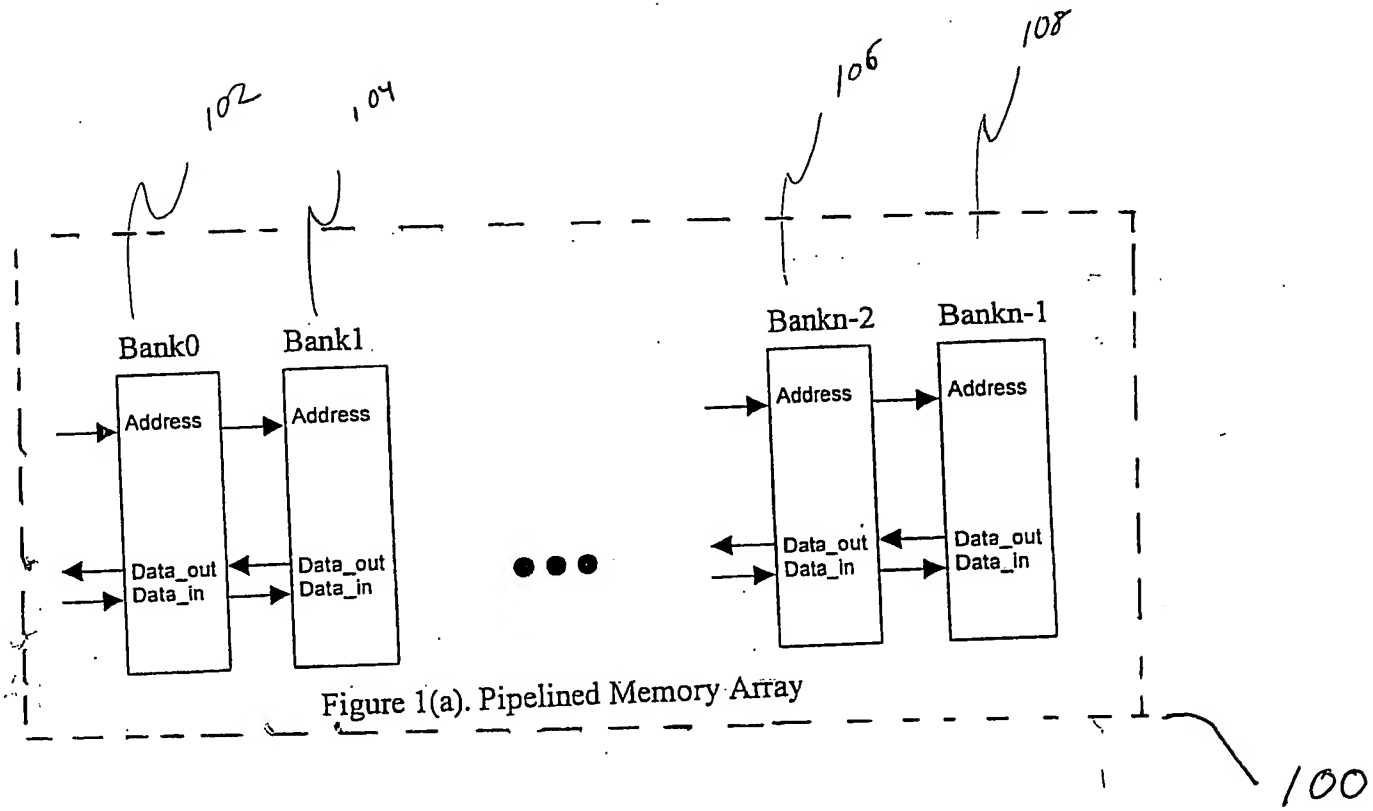


Figure 1(a). Pipelined Memory Array

Figure 1(a)

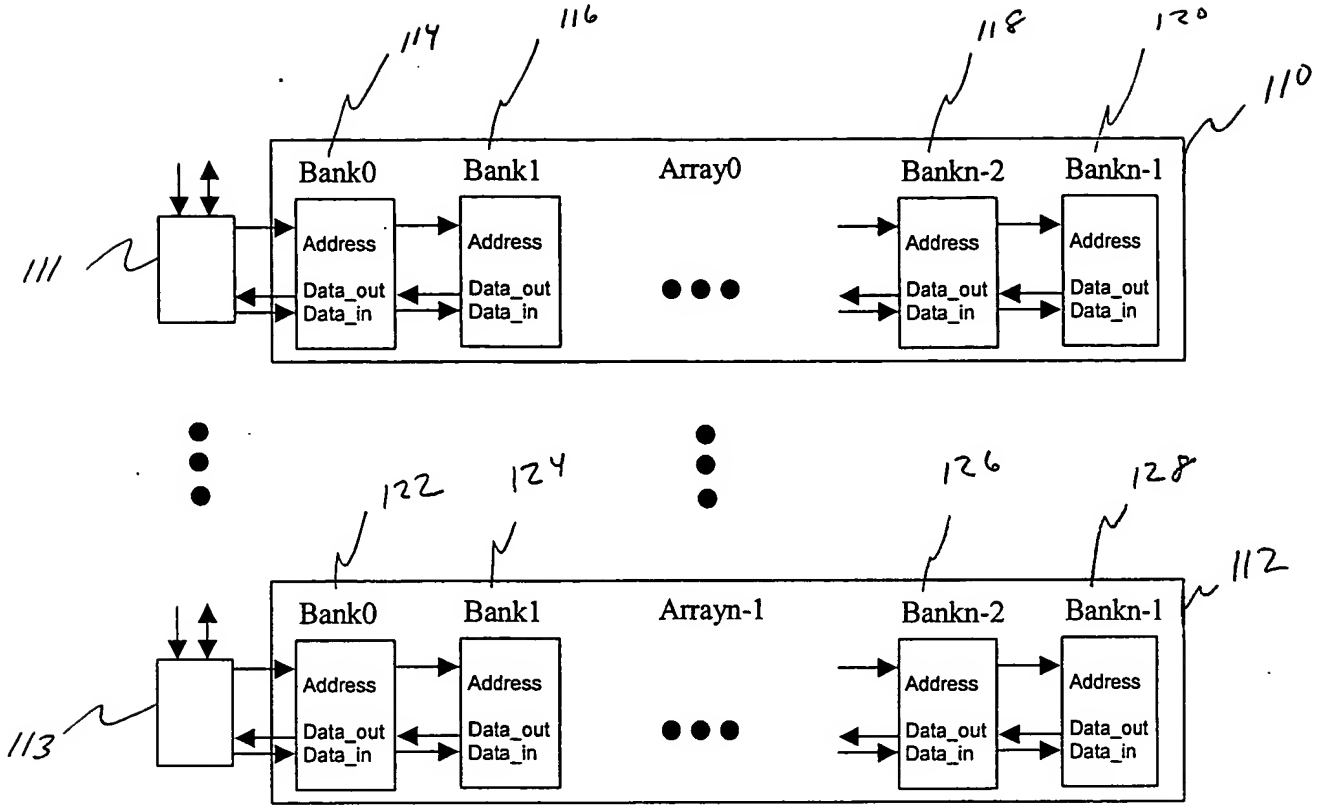


Figure 1(b). Systolic Memory Array

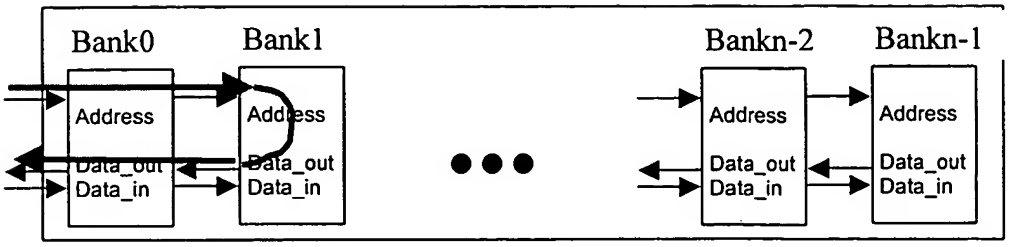


Figure 2(a) Read AdAddress/Data Movement

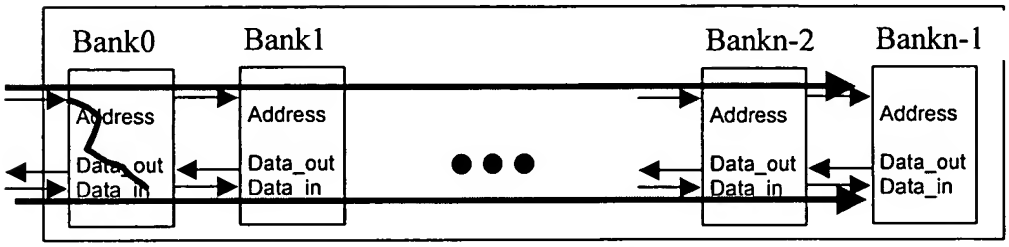


Figure 2(b) Write Address/Data Movement

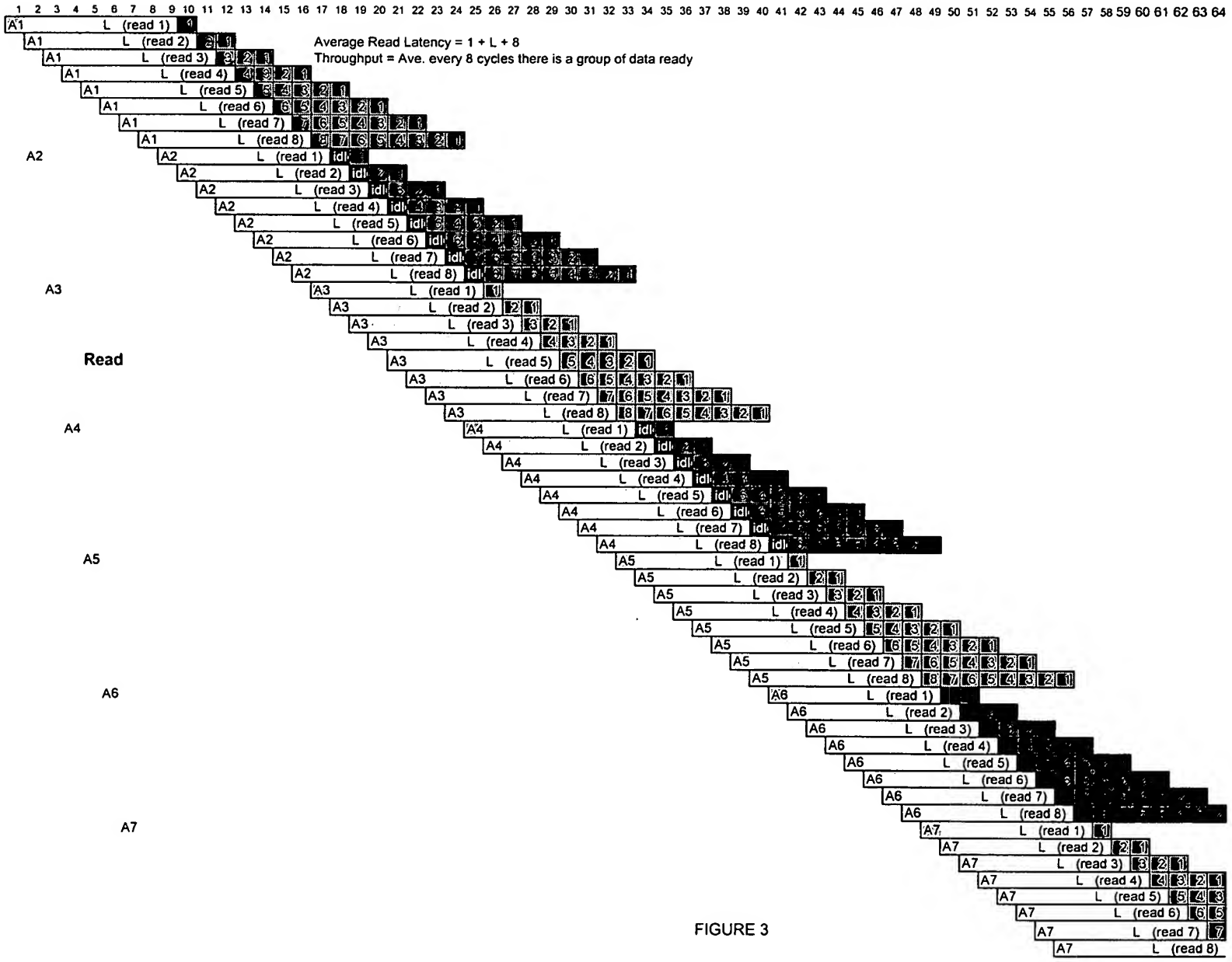


FIGURE 3

BEST AVAILABLE COPY

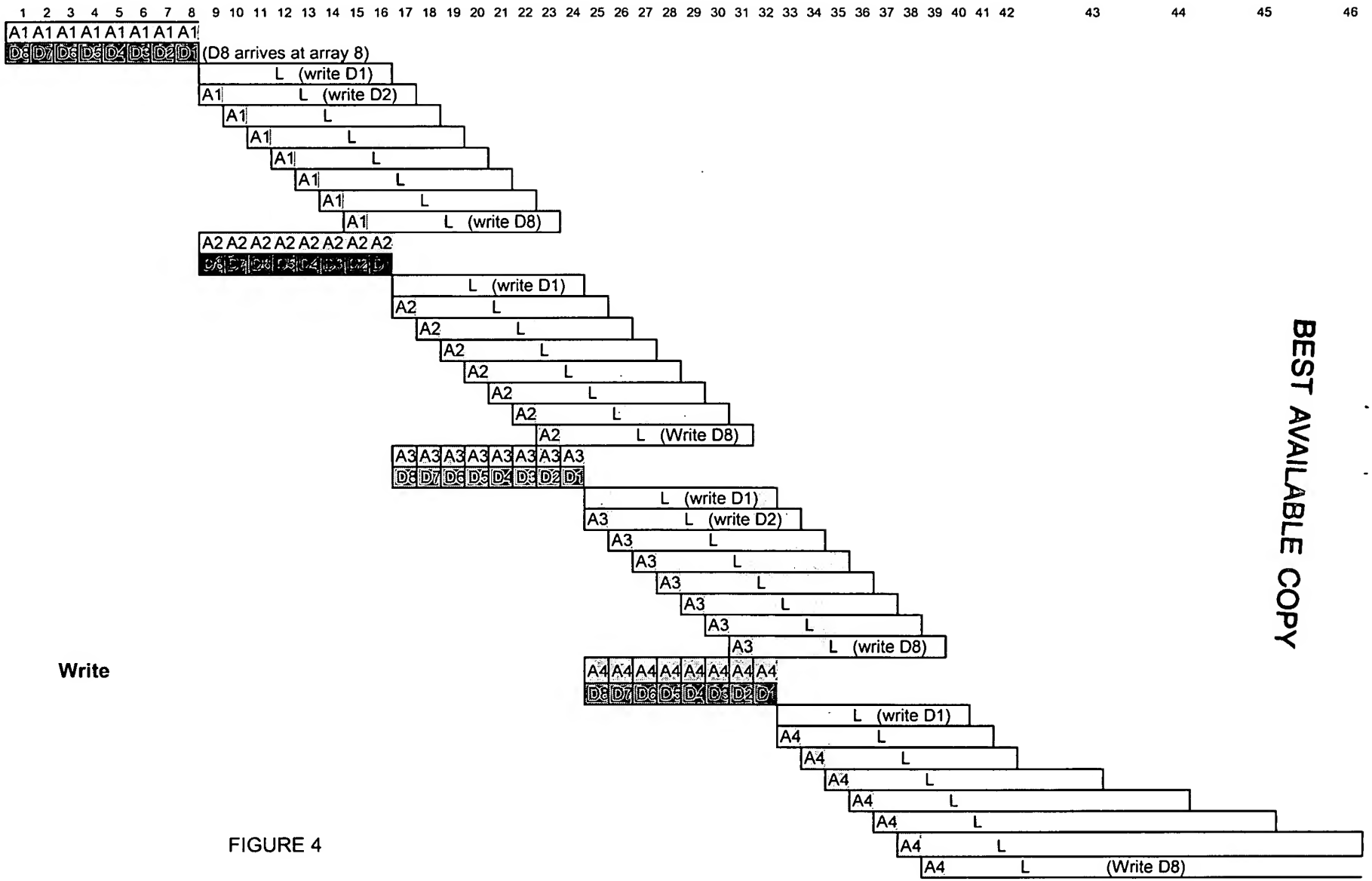
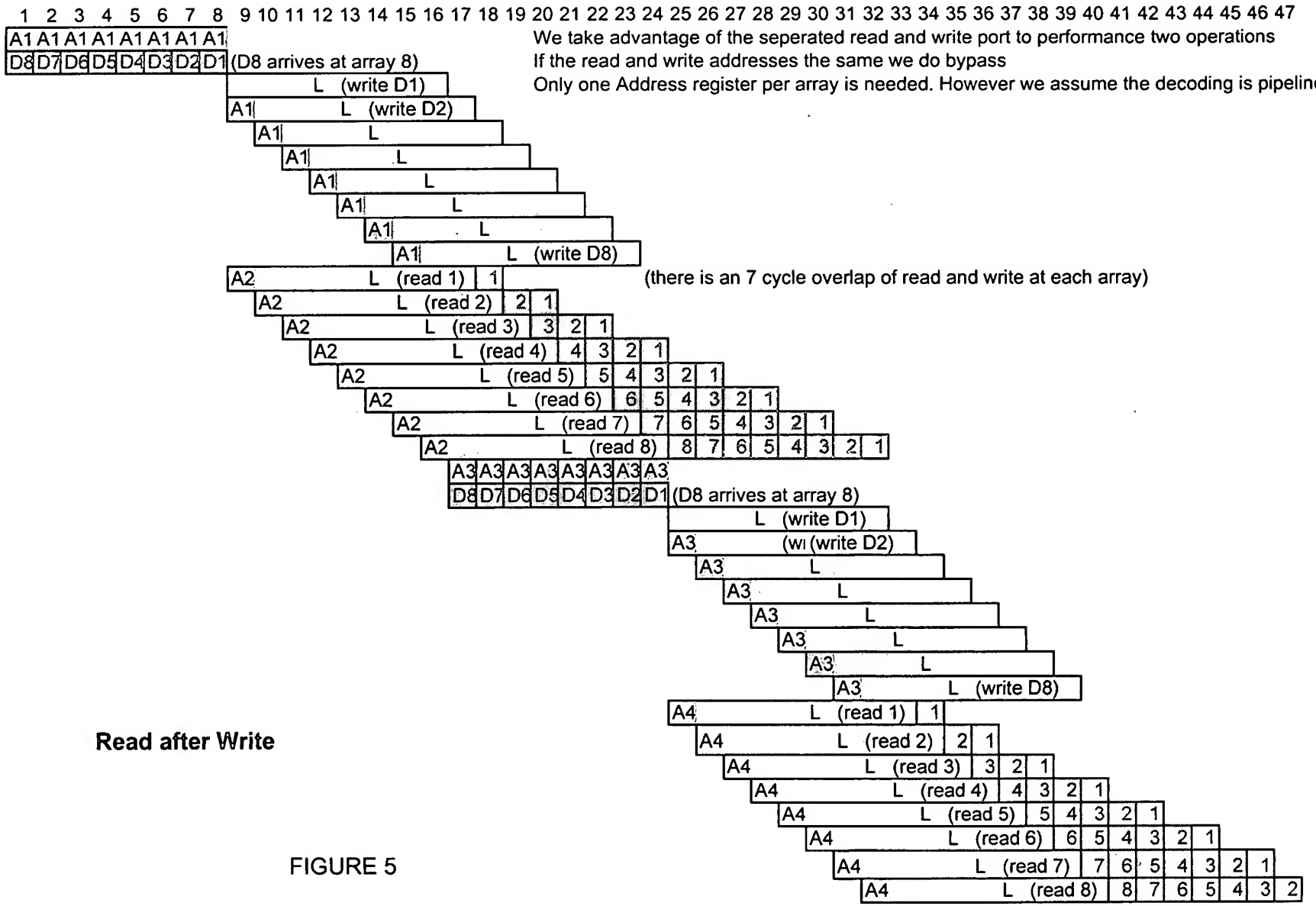


FIGURE 4

BEST AVAILABLE COPY

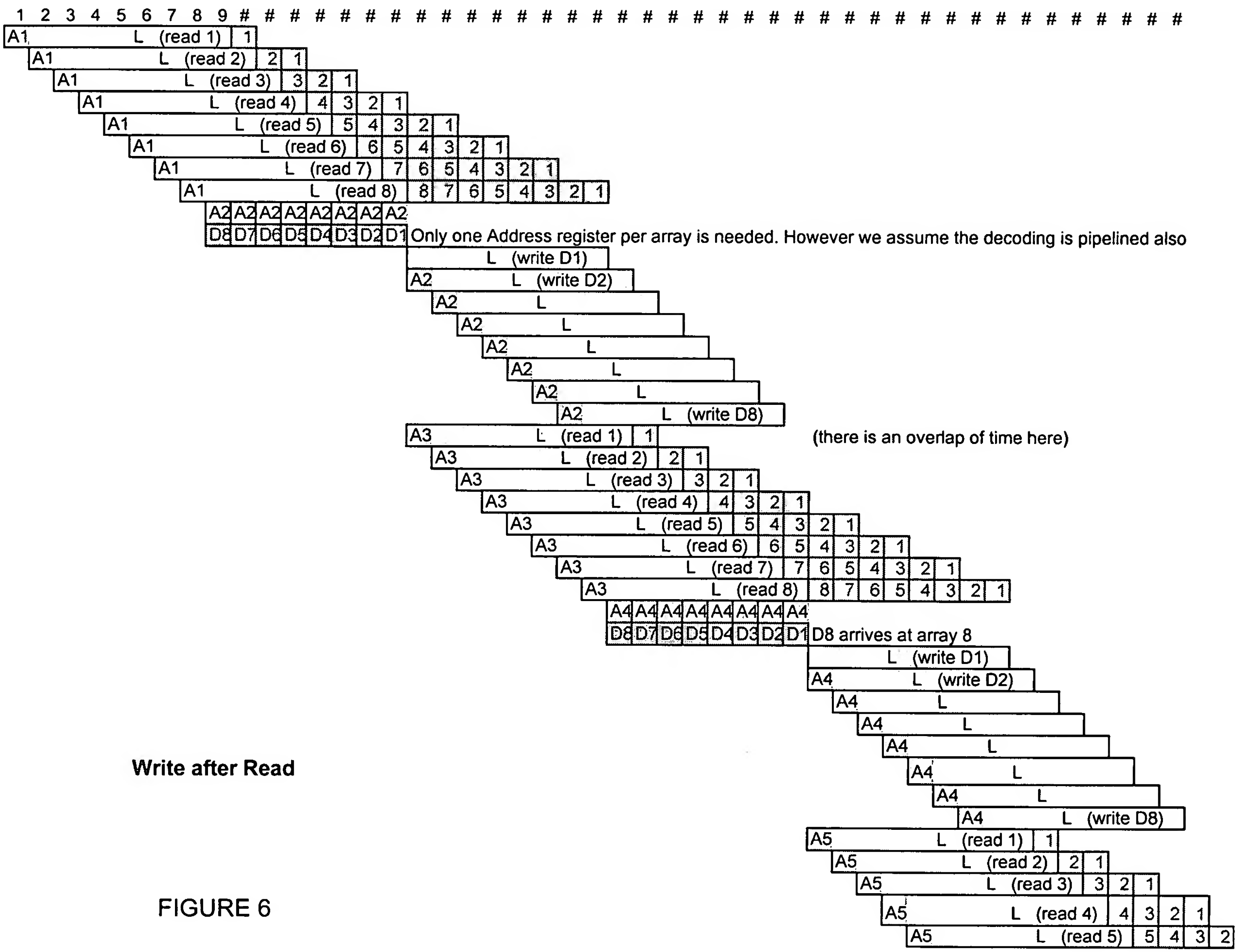


Read after Write

FIGURE 5

BEST AVAILABLE COPY

BEST AVAILABLE COPY



Write after Read

FIGURE 6

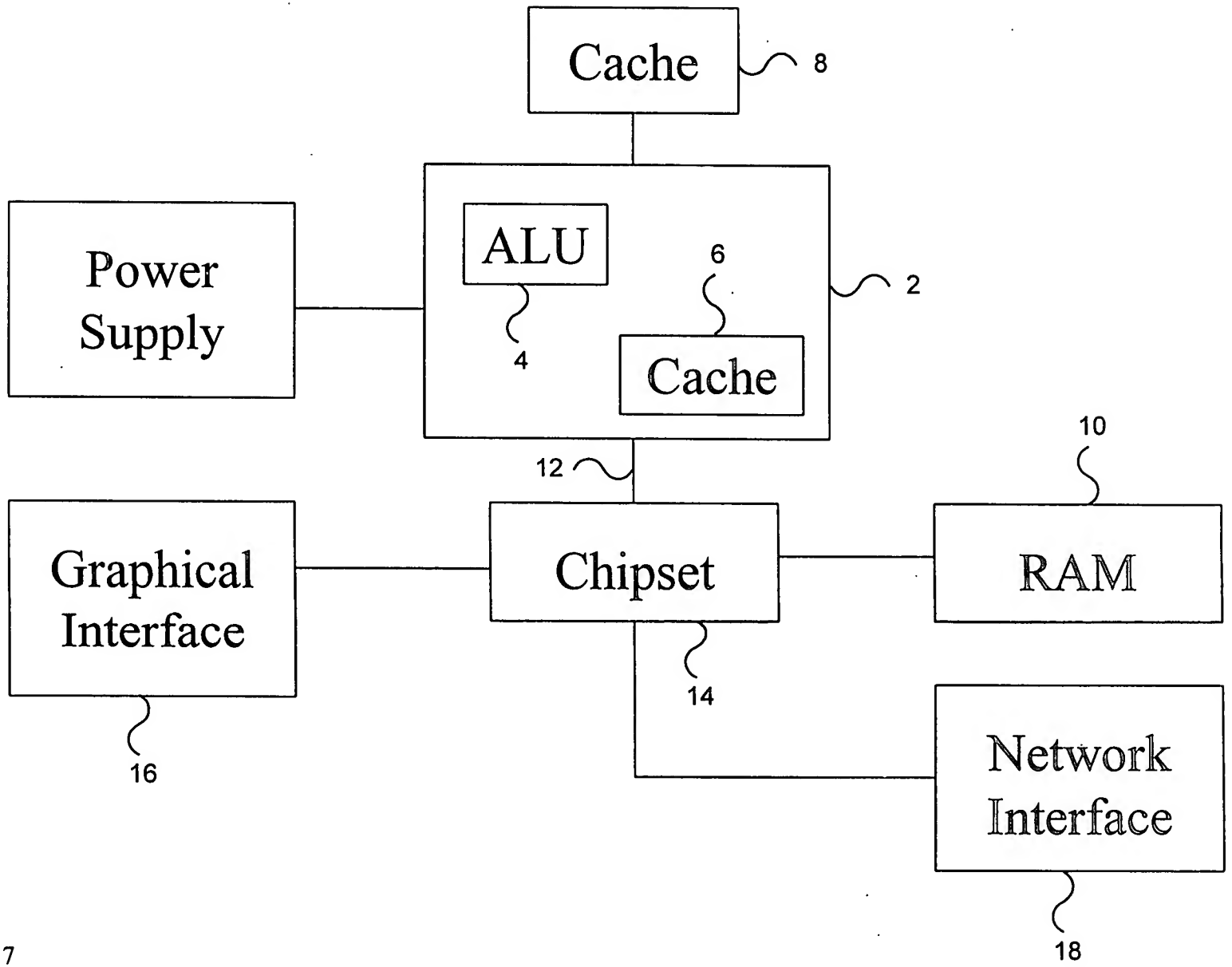

Cache
8
Power Supply
ALU
6
2
4
Cache
10
12
Graphical Interface
Chipset
RAM
14
Network Interface
16
18

Figure 7